REMARKS

Claims 1-10 are pending. Claims 11-18 were previously cancelled with the prior response. Reconsideration of the application is respectfully requested for at least the following reasons.

I. REJECTION OF CLAIMS 1-6, 8, AND 9 UNDER § 102

Claims 1-6, 8, and 9 were rejected under 35 U.S.C. §102(e) as being clearly anticipated by U.S. Patent Publication No. 2004/0062267 (Minami et al.). Withdrawal of the rejection is respectfully requested for at least the following reasons.

i. Minami et al. fail to anticipate a security system configured to send an outgoing data packet to a first and an outgoing data packet to a second processor, as recited in claim 1.

Claim 1 refers to a network interface system comprising a security system configured to send an outgoing data packet to a first processor, then a subsequent outgoing data packet to a second processor, then a further subsequent outgoing data packet to the first processor, and continuing in this alternating manner, for encryption. As will be more fully appreciated below, Minami et al. fail to anticipate a security system configured to ***send an outgoing data packet to a first processor and an outgoing data packet to a second processor.***

Minami et al. teach a security system comprising two parallel and identical encryption engines. (*See,* par. [1746]). Packets are transferred from a memory to the security system, where the encryption engines are "serviced in alternating order". (*See,* par. [1746]). Once serviced the encrypted data is written to the same memory location as the source packet. (*See,* par. [1745]). When an encrypted packet is ready for transmission, an Ethernet transmission arbitrator reads the packet data directly from memory and sends it to a transmit buffer. When the entire packet has been read out of the memory it is transmitted. (*See,* par. [1748]).

The term data packet, as used in claim 1 of the present invention, is well known in the art to refer to a collection of data configured in a structure which comprises a header section and a payload section. Claim 1 requires that a data packet is transferred to a first processor prior to a data packet being transferred to a second processor. This means that ***an entire data packet must be transferred before toggling which encryption engine to send the data to***.

In contrast, Minami et al. teach a module comprising two parallel and identical encryption engines that, "are serviced in alternating order". The phrase "[the parallel encryption engines] are serviced in alternating order" ***is silent in regard to the amount of data that is sent to each encryption engine when an engine is serviced***. Minami merely teaches that the encryption engines are serviced in an alternating order, not that data packets are alternatively sent to a first and a second encryption engine, as recited in claim 1.

Furthermore, the use of a buffer to subsequently transmit an entire data packet from memory, but not in moving data from memory to the parallel encryption engines for servicing, implies that ***an entire packet is not necessarily transferred to a single encryption engine***. The use of a buffer for data packet transmission from memory 675 to module 676 teaches using a buffer for moving an entire data packet from memory to another module. Therefore, not using a buffer to transmit data from memory 675 to module 674 implies that an entire packet is not necessarily transferred to respective encryption engines. Accordingly, Minami et al. fail to specifically teach sending outgoing data packets to a first and a second processor, as recited in claim 1.

Since Minami et al. fail to specifically teach ***sending an outgoing data packet to a first and that an outgoing data packet to a second processor,*** Minami et al. fail to anticipate claim 1 of the present invention. Accordingly, withdrawal of the rejection is respectfully requested.

Claims 2-6, 8, and 9 depend upon claim 1 and add further limitations thereto. Because Minami et al. do not anticipate the present invention of claim 1, claims 2-6, 8,

and 9 are not anticipated by the cited art. Accordingly, withdrawal of the rejection is respectfully requested.

ii. Minami et al. fail to anticipate pipelines for ESP encryption, ESP authentication, and AH authentication, as recited in claim 6.

Claim 6 refers to a network interface system comprising a security system comprising a first and second processor, wherein the processors each comprise pipelines for ESP encryption, ESP authentication, and AH authentication. Minami et al. fail to anticipate processors comprising ***pipelines for*** ESP encryption, ESP authentication, and AH authentication.

The Office Action alleges Minami et al. teach a security system comprising two processors each comprising pipelines for ESP encryption, ESP authentication, and AH authentication in paragraphs 1744-1746, 105, 896, 1605-1622 and throughout the reference. (*See*, p. 5, lns. 3-5). It is conceded that Minami et al. teach ESP protocols for both transmission and reception security, however it is respectfully argued that Minami et al. fail to anticipate ***pipelines for ESP encryption***. Accordingly, withdrawal of the rejection is respectfully requested.

If this argument is not found to be persuasive the applicants ask for further clarification as to Minami et al. anticipating pipelines for ESP encryption.

II. REJECTION OF CLAIMS 4 AND 5 UNDER 35 U.S.C. § 103

Claims 4 and 5 were rejected under 35 U.S.C. §103(a) as being obvious over U.S. Patent Publication No. 2004/0062267 (Minami et al.). Withdrawal of the rejection is respectfully requested for at least the following reasons.

As stated above, Minami et al. do not teach over the invention of independent claim 1. Claims 4 and 5 depend upon claim 1 respectively, and adds further limitations thereto. Because the primary reference does not teach the present invention of claim 1, claims 4 and 5 are also non-obvious over the cited art. Accordingly, withdrawal of the rejection is respectfully requested.

III. REJECTION OF CLAIM 7 UNDER 35 U.S.C. § 103(a)

Claim 7 was rejected under 35 U.S.C. §103(a) as being obvious over U.S. Patent Publication No. 2004/0062267 (Minami et al.) in view of U.S. Patent Publication 2004/0128553 (Buer et al.). Withdrawal of the rejection is respectfully requested for at least the following reasons.

As stated above, Minami et al. do not teach over the invention of independent claim 1. Claim 7 depends upon claim 1, and adds further limitations thereto. Because the primary reference does not teach the present invention of claim 1, and because Buer et al. fail to remedy the deficiencies in the primary reference, claim 7 is also non-obvious over the cited art. Accordingly, withdrawal of the rejection is respectfully requested.

IV. REJECTION OF CLAIM 10 UNDER 35 U.S.C. § 103(a)

Claim 10 was rejected under 35 U.S.C. §103(a) as being obvious over U.S. Patent Publication No. 2004/0062267 (Minami et al.) in view of Patt , Patel, Evers, Friendly, and Start's "One Billion Transistors, One Uniprocessor, One Chip" (Patt et al.). Withdrawal of the rejection is respectfully requested for at least the following reasons.

As stated above, Minami et al. do not teach over the invention of independent claim 1. Claim 10 depends upon claim 1, and adds further limitations thereto. Because the primary reference does not teach the present invention of claim 1, and because Patt et al. fail to remedy the deficiencies in the primary reference, claim 10 is also non-obvious over the cited art. Accordingly, withdrawal of the rejection is respectfully requested.

V. CONCLUSION

For at least the above reasons, the claims currently under consideration are believed to be in condition for allowance.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 50-1733, AMDP751US.

Respectfully submitted,
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